a plurality of word driver circuits each [providing] having an output [voltage to a word line] node coupled to a corresponding one of said plurality of word lines;

a voltage generator circuit supplied with an operating voltage so as to provide a first voltage to said plurality of word driver circuits;

wherein the amplitude of said first voltage is larger than that of said operating voltage so that said plurality of word driver circuits can provide [the] an output voltage at an amplitude larger than an amplitude of an input voltage;

wherein said voltage generator circuit provides a small output current to said plurality of word driver circuits in order to keep [the output voltages] a voltage thereof to the first voltage when none of said plurality of word lines is selected, and provides a large output current to one of said [one of] plurality of word driver circuits in response to a first signal from an outside of the chip;

wherein each of said plurality of word driver circuits brings its associated word line to a predetermined potential lower than said first voltage when said associated word line is not selected; and

wherein each of said plurality of word driver circuits establishes a current path between the first voltage and its associated word line, raising the potential on said associated word line to the first voltage, when said associated word line is selected.

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8 ~~35~~. (Amended) The semiconductor memory according to claim ~~34~~ 7,

wherein said voltage generator circuit has a first operation mode and a second operation mode;

wherein the amount of current supplied when in said first operation mode is larger than that of said [operation second] second operation mode; and

wherein said voltage generator circuit is in said first operation mode when one of said word lines is selected.

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10 ~~37~~. (Amended) The semiconductor memory according to claim ~~34~~ 7,

wherein said voltage generator circuit also includes a voltage clamp circuit, clamping the first voltage to a second predetermined potential, coupled to the second output node.

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14 41. (Amended) The semiconductor memory according to claim 34, wherein the operating voltage is a external voltage which is supplied [form] from an outside of the chip.

15 42. (Amended) A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a plurality of word drivers, each word driver having a first output node coupled to a corresponding one of said plurality of word lines, and a first power receiving node;

a voltage generator circuit having a second output node coupled to the first power receiving nodes of said plurality of word drivers, and a second power receiving node to which an operating voltage is supplied;

wherein said voltage generator circuit produces a first voltage which is larger than the operating voltage both in a first mode when one of said plurality of word lines is selected and in a second mode when none of said plurality of word lines is selected;

wherein each of said plurality of word drivers brings its corresponding word line to a predetermined potential, lower than said first voltage, when said corresponding word line is not selected;

wherein a selected one of said plurality of word drivers establishes a current path between the second output node and the corresponding one of said plurality of word lines, raising the potential on said corresponding one of said plurality of word lines to said first voltage; and

wherein the amount of current supplied when in said first mode is larger than that of said second mode.

23 50. (Amended) A semiconductor memory in a chip, comprising:

plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a first subset of said plurality of dynamic memory cells;

a plurality of data lines, each data line coupled to the source or drain [electrode of one] electrodes of said transfer MOS transistors of a second subset of said plurality of dynamic memory cells;

a plurality of sense amplifiers, each sense amplifiers having a input/output node coupled to a corresponding one of said plurality of data lines;

a plurality of word drivers, each word driver having a first output node coupled to a corresponding one of said plurality of word lines, and a first power receiving node;

a voltage generator circuit having a second output node coupled to the first power receiving node of each of said plurality of word drivers;

a voltage limiter circuit having a third power receiving node to which an external voltage is supplied, and a third output node providing an internal voltage;

wherein said voltage generator circuit produces a first voltage [which is larger than the operating voltage] both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected;

wherein each of said plurality of word drivers brings its corresponding word line to a predetermined potential, lower than said first voltage, when said corresponding word line is not selected;

wherein a selected one of said plurality of word drivers establishes a current path between the second output node and the corresponding one of said plurality of word lines, raising the potential on said corresponding one of said plurality of word lines to said first voltage;

wherein a signal of the corresponding one of said plurality of data lines read from the corresponding one of said plurality of memory cells is amplified to a first potential or second potential by the corresponding one of said plurality of sense amplifiers;

wherein the first potential is larger than the second potential;

wherein the first potential is clamped to a voltage level of the internal voltage, wherein the internal voltage is smaller than the external voltages, and

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wherein a level of the first voltage is larger than the first potential.

24 ~~51~~. (Amended) The semiconductor memory according to claim 23 ~~50~~, wherein said voltage generator circuit has a first operation mode and a second operation mode, the amount of current being supplied by said voltage generator [for circuit] in said first operation mode being more than the amount of current supplied in said second operation mode, and

wherein said voltage generator circuit is in the first operation mode when one of said plurality of word lines is selected.

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39 ~~66~~. (Amended) The semiconductor memory according to claim 36 ~~63~~, wherein the first charge pump circuit produces the first voltage in response to a signal which indicates a start of accessing said plurality of dynamic memory cells.

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41 ~~68~~. (Amended) A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a plurality of word drivers, each word driver having:

a first output node coupled to a corresponding one of said plurality of word lines;

a first power receiving node;

a P-channel MOS transistor having[;]:

a source-drain path which is coupled between the first power receiving node and the first output node; and

a gate electrode coupled to a selection node to which a signal selecting its corresponding word line may be supplied to close said source-drain path;

said first output supplying a predetermined potential, lower than a first voltage, when said corresponding word line is not selected; and

a voltage generator circuit having:

a second output node coupled to the first power receiving nodes of each of said plurality of word drivers:

having a second power receiving node to receive an operating voltage; and

producing, at said second output node, the first voltage which is larger than the supplied operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected for reading

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(Amended) A semiconductor memory in a chip, comprising:

a plurality of dynamic memory cells, each cell including a transfer MOS transistor with a gate electrode and a capacitor;

a plurality of individually selectable word lines, each word line coupled to gate electrodes of the transfer MOS transistors of a subset of said plurality of dynamic memory cells;

a voltage generator circuit:

having a first output node and a first power receiving node to receive an operating voltage; and

producing, at said first output node, a first voltage which is larger than the supplied operating voltage both when one of said plurality of word lines is selected and when none of said plurality of word lines is selected;

a plurality of word drivers, each word driver having:

a second output node coupled to a corresponding one of said plurality of word lines; [and]

a second power receiving node coupled to the first output node;

a P-channel MOS transistor having:

a source-drain path which is coupled between the second power receiving node and the second output node; and

a gate electrode coupled to a selection node to which a signal selecting its corresponding word line may be supplied to close said source-drain path of the P-channel MOS transistor; and